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Methods Of Forming Circuit Traces And Contact Pads For Interposers Utilized In Semiconductor Packages

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INVENTORS

Stephen F. Moxham
Lee Teck Kheng
Steve Thummel

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METHODS OF FORMING CIRCUIT TRACES AND CONTACT PADS FOR INTERPOSERS UTILIZED IN SEMICONDUCTOR PACKAGES

TECHNICAL FIELD

[0001] The present invention pertains to methods of fabricating circuit traces and contact pads for interposers utilized in semiconductor packages.

BACKGROUND OF THE INVENTION

[0002] Semiconductor devices, for example, dynamic random access memory (DRAM) devices, are shrinking in the sense that smaller devices are being manufactured that are able to handle larger volumes of data at faster data transfer rates. As a result, semiconductor manufacturers are moving toward chip-scale packages (CSP) for semiconductor components which have a small size and fine pitch wiring.

[0003] Exemplary CSPs are shown in Figs. 1 and 2 as a flip-chip-in-package-board-on-chip (FCIP-BOC) package 10 and a board-on-chip BOC package 50, respectively. Each of the packages comprises a semiconductor component 12 (such as, for example, an integrated circuit (IC) chip), and can thus be referred to as semiconductor packages.

[0004] The packages 10 and 50 also comprise an interposer 14 utilized to support the semiconductor component 12. The shown interposer is a board, and such board would typically be a glass weave material. In the case of BOC construction 50, chip 12 is attached to board 14 through an adhesive 16. In the case of FCIP-BOC construction 10, the attachment between the chip 12 and board 14 is through a series of electrical contacts 18 and/or 36. Each of the illustrated contacts 18 comprises an electrically conductive interconnect material

20 (shown as a small ball) between a pair of contact pads 22 and 24. The contact pad 22 is associated with chip 12, and the contact pad 24 is associated with board 14. Contact pad 24 will typically comprise a stack of a copper layer, nickel layer and gold layer; with the copper layer being adjacent board 14 and the gold layer being adjacent ball 20 of interconnect 18. Contact pads 22 can comprise constructions analogous to those of contact pads 24.

[0005] Constructions 10 and 50 are shown comprising contact pads 30 on an underside of the board 14 (i.e., on a side of board 14 in opposing relation relative to the side proximate chip 12), and comprising electrically conductive interconnect material (shown as solder balls 32) on the contact pads 30. Contact pads 30 can comprise constructions analogous to those described above with reference to pads 24, and accordingly can comprise stacks of copper, nickel and gold. Solder balls 32 are utilized to form electrical interconnections between contact pads 30 and other circuitry (not shown) external of the chip package (i.e., the package 10 or the package 50).

[0006] The boards 14 have orifices 34 extending therethrough. Wire bonds 36 extend from contact pads 38 associated with chips 12 to contact pads 40 associated with an underside of board 14. The contact pads 40 can be connected with pads 30 through circuit traces (not shown in the views of Figs. 1 and 2). The FCIP-BOC construction 10 also comprises conductive vias 42 extending through board 14 to connect selected contact pads 24 above the board with selected contact pads 30 beneath the board.

[0007] Suitable encapsulant 44 can be provided over the chip 12, around the wire bonds 36, and within orifice 34 as shown.

[0008] From the discussion above it can be recognized that FCIP-BOC construction 10 is similar to BOC construction 50, with the primary differences being that FCIP-BOC construction 10 comprises contacts formed both above and below board 14 (i.e., on opposing surfaces of board 14), whereas BOC construction 50 has contacts formed only beneath board 14.

[0009] The invention described herein includes methods of forming boards and other interposers utilized in semiconductor packages. The methods can be utilized in, for example, forming either FCIP-BOC constructions or BOC constructions. Before discussing the methods of the present invention, a problem associated with prior art fabrication of boards is described with reference to Figs. 3-9. The figures show an exemplary process for forming a board of a BOC construction, but it is to be understood that similar methodology is utilized for forming boards utilized in FCIP-BOC constructions, and accordingly problems similar to those described with reference to Figs. 3-9 also occur in forming boards associated with FCIP-BOC constructions.

[0010] Referring to Figs. 3 and 4, a construction 51 is shown at a preliminary stage of a prior art process of fabricating the board for utilization in a BOC construction. The construction is shown in a cross-sectional view in Fig. 3, and in a top view in Fig. 4.

[0011] Construction 51 includes a board 14. Board 14 comprises a first surface 15 and a second surface 17 in opposing relation to first surface 15. A conductive layer 52 is provided over first surface 15. Conductive layer 52 will typically comprise, for example, copper, and can have an initial thickness of greater than 10 microns, with a typical thickness being about 12 microns. Since the shown board is to be utilized for forming a BOC construction, conductive

layer 52 is only along one of the surfaces 15 and 17. However, if board 14 were to be utilized in forming a FCIP-BOC construction, the conductive material would be formed along both of surfaces 15 and 17.

[0012] Figs. 5 and 6 show construction 51 at a processing stage subsequent to that of Figs. 3 and 4 along cross-sectional and top views, respectively. Layer 52 is patterned into a series of circuit traces 54. It is noted that an alternative route to obtain the construction of Figs. 5 and 6, other than that shown in Figs. 3-6, is to start with a construction having conductive material 52 over both of opposing sides 15 and 17 at the processing stage of Fig. 3, and to etch the conductive material from over side 17 while forming the traces 54 of Figs. 5 and 6.

[0013] Figs. 7 and 8 show construction 51 at a processing stage subsequent to that of Figs. 5 and 6, along cross-sectional and top views, respectively. A series of conductive busses 56 (shown in Fig. 8) are formed across upper surface 15 of board 14, and utilized to form electrical connections to traces 54. Subsequently, a patterned mask (not shown) is formed over portions of traces 54 while leaving portions 62 exposed for formation of contact pads 30. Contact pads are formed electrolytically. Specifically, busses 56 are connected to a power source (not shown), and subsequently conductive layers 58 and 60 are plated onto the contact pad locations of traces 54 to form the contact pads 30. Layers 58 and 60 can comprise, consist essentially of, or consist of, for example, nickel and gold, respectively; and can be referred to as a nickel-containing layer and a gold-containing layer, respectively.

[0014] Fig. 9 shows a top view of construction 51 in a processing stage subsequent to that of Fig. 8. Specifically, orifice 34 has been formed to extend

through board 14. Orifice 34 can be formed utilizing, for example, a router. The forming of orifice 34 removes the majority of busses 56 from board 14. However, remaining portions of busses 56 can problematically leave burrs 70 along edges of orifice 34. Also, the busses can have a so-called "antenna effect" on high speed traces, which can impair high frequency electrical performance.

[0015] Other problems of prior art processes of forming conductive traces and contact pads for board substrates can include utilization of unstable plating solutions, poor wirebondability, slow plating processes, difficulty in achieving thick platings, and high cost due to, among other things, complexities of incorporating busses into design space.

[0016] In light of the above-discussed problems, it is desirable to develop new methods of forming interposers suitable for incorporation into semiconductor packages.

SUMMARY OF THE INVENTION

[0017] In one aspect, the invention encompasses a method of forming circuit traces and contact pads for an interposer utilized in a semiconductor package. An interposer substrate having a pair of opposing surfaces is provided. The opposing surfaces are defined as a first surface and a second surface, and the substrate has a first conductive material extending at least over the first surface. Pads are formed over the first conductive material by plating a second conductive material over the first conductive material while using the first conductive material as an electrical connection to a power source. After the plating, the first conductive material is patterned into electrical traces. The

semiconductor package can be, for example, either a FCIP-BOC construction or a BOC construction.

[0018] In one aspect, the invention encompasses a method for forming a BOC package. An interposer substrate (in this case a board substrate), is provided. The substrate has a surface, and a first conductive layer over such surface. A first patterned mask is formed over the first conductive layer. The first patterned mask has openings extending therethrough to the first conductive layer, with the openings defining circuit trace locations. A second conductive layer is formed over and in physical contact with portions of the first conductive layer exposed through the openings. The second conductive layer is thus formed at the circuit trace locations, and is formed in a circuit trace pattern. A second patterned mask is formed to cover regions of the first conductive layer while leaving other regions exposed. The exposed regions define contact pad locations. Conductive materials are plated over the contact pad locations, and the first and second patterned masks are then removed. The circuit trace pattern is then transferred to the first conductive layer with a suitable etch.

[0019] In one aspect, the invention encompasses a method of forming a board for utilization in a FCIP-BOC package. A board substrate is provided. The substrate has a pair of opposing surfaces, with the opposing surfaces being defined as a first surface and a second surface. A first conductive layer is formed over the first surface, and a second conductive layer is formed over the second surface. A first patterned mask is formed over the first and second conductive layers. The first patterned mask has openings extending therethrough to the first and second conductive layers. The openings define contact pad locations. A third conductive layer is formed over and in physical

contact with portions of the first and second conductive layers exposed through the openings. The third conductive layer is thus formed at the contact pad locations. The first patterned mask is removed. A second patterned mask is then formed over the first and second conductive layers. The second patterned mask protects regions of the first and second conductive layers while exposing other regions. The protected regions define circuit traces to at least some of the contact pad locations. Unprotected regions of the first and second conductive layers are removed to form the circuit traces from the first and second conductive layers. Subsequently, the second patterned mask is removed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0021] Fig. 1 is a diagrammatic cross-sectional side view of a prior art FCIP-BOC semiconductor package construction.

[0022] Fig. 2 is a diagrammatic cross-sectional side view of a prior art board-on-chip semiconductor package construction.

[0023] Figs. 3 and 4 are a diagrammatic cross-sectional side view, and a diagrammatic top view, respectively, of a board construction at a preliminary processing stage of a prior art method for fabricating a board for inclusion within a semiconductor package. The cross-section of Fig. 3 is shown along the line 3-3 of Fig. 4.

[0024] Figs. 5 and 6 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the board construction of Figs. 3 and 4

shown at a prior art processing stage subsequent to that of Figs. 3 and 4. The cross-section of Fig. 5 is shown along the line 5-5 of Fig. 6.

[0025] Figs. 7 and 8 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the board construction of Figs. 3 and 4, shown at a prior art processing stage subsequent to that of Figs. 5 and 6. The cross-section of Fig. 7 is shown along the line 7-7 of Fig. 8.

[0026] Fig. 9 is a top view of the board construction of Figs. 3 and 4 shown at a prior art processing stage subsequent to that of Figs. 7 and 8.

[0027] Fig. 10 is a diagrammatic cross-sectional side view of a board construction shown at a preliminary processing stage of a method of the present invention.

[0028] Figs. 11 and 12 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a processing stage subsequent to that of Fig. 10. The cross-section of Fig. 11 is shown along the line 11-11 of Fig. 12.

[0029] Figs. 13 and 14 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a processing stage subsequent to that of Figs. 11 and 12. The cross-section of Fig. 13 is shown along the line 13-13 of Fig. 14.

[0030] Figs. 15 and 16 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a processing stage subsequent to that of Figs. 13 and 14. The cross-section of Fig. 15 is shown along the line 15-15 of Fig. 16.

[0031] Figs. 17 and 18 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a

processing stage subsequent to that of Figs. 15 and 16. The cross-section of Fig. 17 is shown along the line 17-17 of Fig. 18.

[0032] Figs. 19 and 20 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a processing stage subsequent to that of Figs. 17 and 18. The cross-section of Fig. 19 is shown along the line 19-19 of Fig. 20.

[0033] Figs. 21 and 22 are a diagrammatic cross-sectional side view and a diagrammatic top view, respectively, of the construction of Fig. 10 shown at a processing stage subsequent to that of Figs. 19 and 20. The cross-section of Fig. 21 is shown along the line 21-21 of Fig. 22.

[0034] Fig. 23 is a diagrammatic top view of the Fig. 10 construction shown at a processing stage subsequent to that of Figs. 21 and 22.

[0035] Fig. 24 is a diagrammatic top view of the construction of Fig. 10 shown at a processing stage subsequent to that of Fig. 23.

[0036] Fig. 25 is a diagrammatic top view of a panel comprising a plurality of board constructions which can be processed simultaneously.

[0037] Figs. 26, 27 and 28 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of a board construction at a preliminary processing stage of forming a board suitable for utilization in an FCIP-BOC construction in accordance with an aspect of the present invention. The cross-section of Fig. 26 is along the lines 26-26 of Figs. 27 and 28.

[0038] Figs. 29, 30 and 31 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of

Figs. 26-28. The cross-section of Fig. 29 is shown along the lines 29-29 of Figs. 30 and 31.

[0039] Figs. 32, 33 and 34 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of Figs. 29-31. The cross-section of Fig. 32 is shown along the lines 32-32 of Figs. 33 and 34.

[0040] Figs. 35, 36 and 37 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of Figs. 32-34. The cross-section of Fig. 35 is shown along the lines 35-35 of Figs. 36 and 37.

[0041] Figs. 38, 39 and 40 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of Figs. 35-37. The cross-section of Fig. 38 is shown along the lines 38-38 of Figs. 39 and 40.

[0042] Figs. 41, 42 and 43 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of Figs. 38-40. The cross-section of Fig. 41 is shown along the lines 41-41 of Figs. 42 and 43.

[0043] Figs. 44, 45 and 46 are a diagrammatic cross-sectional side view, diagrammatic top view and diagrammatic bottom view, respectively, of the board construction of Figs. 26-28 shown at a processing stage subsequent to that of

Figs. 41-43. The cross-section of Fig. 44 is shown along the lines 44-44 of Figs. 45 and 46.

[0044] Fig. 47 shows a processor system including a semiconductor package formed in accordance with methodologies of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0045] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0046] The invention includes methods for forming interposer substrates (e.g., board substrates) suitable for utilization in semiconductor packages. The methods eliminate the bus lines traditionally used during the plating of conductive materials at contact pad locations. The elimination of the bus lines can simplify fabrication relative to prior art processes, in that it eliminates the processing steps utilized for forming the bus lines. Also, it can eliminate problems associated with residual bus lines in conventional processing, such as, for example, the burrs described with reference to prior art Fig. 9, and the antenna effect described in the "Background" section of this disclosure.

[0047] Methodologies of the present invention are suitable for forming interposers (for example, boards, lead-frames, etc.) suitable for utilization in a diverse array of semiconductor packages. Exemplary packages include FCIP-BOC constructions, BOC constructions and chip-on-board (COB) constructions. The exemplary applications which follow utilize board substrates for fabrication of exemplary BOC and FCIP-BOC constructions, but it is to be understood that the invention can be utilized for forming packages other than BOC and FCIP-

BOC constructions, and that the methodology described herein can be utilized with other interposer substrates besides board substrates.

[0048] Figs. 10-24 pertain to a first embodiment of the invention, and Figs. 26-46 pertain to a second embodiment of the invention. The first embodiment is described with reference to a board suitable for utilization in a BOC construction, and the second embodiment is described with reference to a board suitable for utilization in a FCIP-BOC construction. In referring to the embodiments that follow, similar numbering will be used as was utilized in describing the prior art of Figs. 1-9, where appropriate.

[0049] Referring initially to Fig. 10, a board construction 51 is illustrated at a preliminary processing stage of a method of the present invention. Construction 51 of Fig. 10 is similar to the construction described previously with reference to Fig. 3, and accordingly comprises a layer 52 of conductive material over a surface 15 of a substrate 14. Layer 52 can comprise, consist essentially of, or consist of copper. In particular aspects, layer 52 can predominately comprise copper, with the term "predominately comprise" indicating that the layer comprises more than 50 atomic% copper.

[0050] Layer 52 can be initially provided to a thickness of at least about 10 microns, with a typical thickness being about 12 microns. Layer 52 can be referred to as a first conductive layer in the discussion that follows to distinguish layer 52 from subsequent conductive layers formed thereover.

[0051] Referring to Figs. 11 and 12, layer 52 is thinned. The thickness of layer 52 can be reduced to less than or equal to about 5 microns, and typically will be reduced to about 3 microns. Fig. 12 shows that the conductive layer can

extend across an entirety of a surface of substrate 14 (the substrate is visible in the cross-sectional view of Fig. 11).

[0052] Referring to Figs. 13 and 14, a patterned mask 100 is formed over conductive layer 52. Patterned mask 100 can be formed from, for example, a dry film provided over layer 52 and subsequently photolithographically patterned. Openings 102 extend through patterned mask 100 to conductive layer 52. The openings 102 define a circuit pattern.

[0053] Referring to Figs. 15 and 16, a second conductive layer 104 is grown over first conductive layer 52 within openings 102. Second conductive layer 104 can be formed by, for example, electrolytic processing, and accordingly can be plated over first conductive layer 52. In particular aspects, second conductive layer 104 will comprise, predominately comprise, consist essentially of, or consist of, copper. Accordingly, second conductive layer 104 can be substantially identical in composition to first conductor layer 52, and specifically, layers 52 and 104 can both predominately comprise, consist essentially of, or consist of copper.

[0054] Second conductive layer 104 can be formed to a thickness of at least about 10 microns, and in particular aspects will be formed to a thickness of at least about 12 microns. In some aspects, a combined thickness of layers 52 and 104 can be greater than about 10 microns, and in particular aspects the combined thickness can be about 12 microns. Second conductive layer 104 is formed in physical contact with first conductive layer 52, and is formed in the circuit pattern defined by openings 102.

[0055] Referring to Figs. 17 and 18, a second patterned mask 106 is formed over first patterned mask 100 and over portions of the circuit pattern

defined by first patterned mask 100, while leaving some portions of the circuit pattern exposed. The covered portions are labeled 108 in Fig. 18, and the openings extending through second mask 106 are labeled 110. The covered portions of the circuit pattern are shown in dashed line in the top view of Fig. 18 to indicate that such portions are under mask 106, while the exposed portions are shown surrounded by a solid-line periphery. Although second mask 106 is shown formed over first mask 100, it is to be understood that the invention includes other aspects (not shown) in which mask 100 is removed prior to forming mask 106.

[0056] The openings 110 extending through mask 106 can be considered to define contact pad locations, and the portions of second conductive layer 104 exposed through openings 110 can be considered to correspond to the contact pad locations.

[0057] Materials 58 and 60 are formed over the portions of second conductive layer 104 exposed within openings 110 of second patterned mask 106 (i.e., are plated over the contact pad locations), and form contact pads 30. Materials 58 and 60 can be referred to as a third conductive layer and a fourth conductive layer, respectively, in the discussion and claims that follow. Materials 58 and 60 can correspond to the same materials traditionally utilized in contact pads. Accordingly, material 58 can comprise, consist essentially of, or consist of nickel; and material 60 can comprise, consist essentially of, or consist of gold. In some applications, layer 60 can be omitted; and in some applications, one or both of layers 58 and 60 can predominately comprise an element selected from the group consisting of palladium, nickel and gold.

[0058] Layers 58 and 60 can be formed electrolytically over conductive material 104. Specifically, materials 58 and 60 can be plated over conductive material 104 while providing electrical power to the conductive material 104. Electrical power can be provided from a source 112 connected to conductive layer 52. In particular aspects of the present invention, conductive layer 52 will be the only conductive interconnect (i.e., bus) extending across substrate 14 between layer 104 and power source 112. In other words, the bus lines 56 described above with reference to Figs. 8 and 9 are eliminated. The plating solutions utilized during plating of materials 58 and 60 can be chosen for appropriate chemical stability.

[0059] Referring to Figs. 19 and 20, first and second patterned masks 100 and 106 (Figs. 17 and 18) are removed.

[0060] Referring next to Figs. 21 and 22, layers 104, 58 and 60 are utilized as a patterned mask during an etch of first conductive layer 52. Such patterns first conductive layer 52 into electrical traces aligned with the materials of layers 104, 58 and 60 thereover. In the shown aspect of the invention, the traces have the rectangular shapes visible in the top view of Fig. 22 as combinations of materials 104 and 60, with the individual discrete traces being labeled as 118 in Fig. 22.

[0061] Referring to Fig. 23, a patterned mask 120 is formed over construction 51 to cover portions 122 of traces 118 (the covered portions are shown in phantom, dashed-line view in Fig. 23), while leaving contact pads 30 exposed. Mask 120 can be referred to as a solder mask, and is utilized to define locations where solder balls are to be provided in a ball grid array. Such locations correspond to the locations of contact pads 30. As will be understood

by persons of ordinary skill in the art, the openings extending to contact pads 30 can expose the entire area of the contact pads, or can expose only a portion of the area of the contact pads, depending on whether the pads are to be utilized in solder mask defined (SMD) applications or non-solder mask defined (NSMD) applications.

[0062] Referring to Fig. 24, orifice 34 is formed to extend entirely through substrate 14 (visible in the cross-sectional view of Fig. 21) of construction 51. Mask 120 preferably remains in place during formation of orifice 34. Subsequent to the formation of orifice 34, construction 51 can be incorporated into a semiconductor package, such as, for example, the package 50 shown in Fig. 2.

[0063] An advantage of the processing of Figs. 10-24 relative to the prior art processing of Figs. 2-9, is that the bus lines 56 (Figs. 8 and 9) have been eliminated from the processing of the present invention. Accordingly, orifice 34 can be formed without formation of the burrs 70 described above with reference to Fig. 9. Other difficulties associated with busses (such as, for example, the antenna effect of the busses) can also be eliminated.

[0064] The construction of Fig. 24 can be considered to comprise a central region within which orifice 34 is formed, and a peripheral region surrounding the central region. The circuit traces 118 can be considered to be formed in the peripheral region in the shown embodiment. A dashed line 130 is shown in Fig. 24 as an exemplary demarcation between the central region and the peripheral region. One aspect of the invention is that layers 58 and 60 (shown for example in Fig. 22) have been plated over contact locations 30 by using conductive layer 52 (shown in Fig. 17) as an electrical connection to a power source (112 in Fig. 17) and without utilizing conductive busses, other than

the conductive layer 52, extending over any part of the central region of the substrate.

[0065] Although the processing of Figs. 10-24 is described with reference to formation of an individual board construction, it is to be understood that methodology of the present invention can be utilized to form multiple board constructions simultaneously. Fig. 25 shows an exemplary panel 150 at a processing step comparable to that of Figs. 11 and 12. Panel 150 comprises a base 14 (not visible in the top view of Fig. 25) and a conductive layer 52 over the base. A plurality of board locations 51 are defined across panel 150, and each of the board locations 51 can correspond to an individual board construction of the type described in Figs. 10-24. All of the boards associated with the panel can be simultaneously subjected to the processing of Figs. 10-24. During the processing of Fig. 17, electrical power can be provided to layer 52 by providing an electrical contact to the layer at, for example, one or more of the edges of panel 150.

[0066] Although the individual board constructions 51 associated with panel 150 are shown separated from one another in the illustration, it is to be understood that the board constructions can be packed tightly together without intervening spaces between adjacent board constructions in other applications (not shown) to increase the number of board constructions formed from an individual panel.

[0067] The next embodiment of the invention is described initially with reference to Figs. 26-28. Such show a construction 200 comprising the substrate 14 having opposing surfaces 15 and 17. Surfaces 15 and 17 can be referred to as first and second surfaces, respectively. A first conductive layer

202 is provided over first surface 15, and a second conductive layer 204 is provided over second conductive surface 17. Conductive layers 202 and 204 can comprise, consist essentially of, or consist of copper. In particular aspects, layers 202 and 204 will predominately comprise copper. Layers 202 and 204 can thus have compositions identical to the composition of the layer 52 described above with reference to Fig. 10. Layers 202 and 204 can each have thicknesses greater than about 10 microns, and in particular aspects will have thicknesses of about 12 microns. As discussed in the brief description of the drawings, Figs. 27 and 28 correspond to a top view and a bottom view, respectively, of a construction comprising the cross-section of Fig. 26.

[0068] Referring next to Figs. 29-31, openings 206 are formed through substrate 14 together with layers 202 and 204, and subsequently a conductive material 208 is formed within the openings. Openings 206 can be formed by, for example, drilling. Although the openings 206 are shown formed entirely through substrate 14 and layers 202 and 204, it is to be understood that the invention encompasses other aspects (not shown) in which one or more of the openings extend only partially through one or more of substrate 14 and layers 202 and 204. Conductive material 208 can comprise, consist essentially of, or consist of, for example, copper. The openings 206 can ultimately be utilized to form vias, such as, for example, the vias 42 described with reference to prior art Fig. 1. It is to be understood that the vias are optional relative to processing of the present invention, and accordingly can be eliminated in other aspects (not shown).

[0069] Referring next to Figs. 32-34, patterned masks 210 and 212 are formed over exposed surfaces of conductive layers 202 and 204, respectively. Mask 210 has openings 214, 215, 216 and 217 formed therethrough; and mask

212 has openings 218, 219, 220 and 221 formed therethrough. Masks 210 and 212 can correspond to, for example, dry films patterned by photolithography. Openings 218, 219, 220 and 221 are extended into layer 204 (shown in the cross-sectional view of Fig. 32, and specifically shown relative to openings 218 and 220), and openings 214, 215, 216 and 217 are not extended into layer 202. The extension of openings 218, 219, 220 and 221 into layer 204 can be accomplished with a suitable timed etch of the material of layer 204.

[0070] Referring next to Figs. 35-37, conductive materials 58 and 60 are formed within openings 214, 215, 216, 217, 218, 219, 220 and 221. Conductive materials 58 and 60 can comprise the same materials described previously with reference to Fig. 17. Accordingly, conductive material 58 can comprise, consist essentially of, or consist of nickel; and conductive material 60 can comprise, consist essentially of, or consist of gold. Conductive materials 58 and 60 form contact pads, and openings 214, 215, 216, 217, 218, 219, 220 and 221 therefore correspond to contact pad locations.

[0071] Conductive materials 58 and 60 can be formed over conductive layers 202 and 204 utilizing an electrolytic process. Specifically, a power source 222 is connected to layers 202 and 204. The power source is then utilized to provide electrical power to layers 202 and 204 while conductive materials of layers 58 and 60 are electrolytically formed (i.e., plated) within openings 214, 215, 216, 217, 218, 219, 220 and 221. The plating solutions utilized during plating of materials 58 and 60 can be chosen for appropriate chemical stability.

[0072] It is noted that layer 58 is shown inset within layer 204 in openings 218 and 220, and is shown on an upper surface of layer 202 within openings 214 and 216. Layer 58 can be inset within an underlying conductive layer if a

suitable etch is performed to form an opening extending into such layer (described above with reference to Figs. 32-34). Alternatively if no such suitable etch is performed, layer 58 will be formed over an exposed upper surface of the conductive layer. In the shown aspect of the invention, layer 204 has been subjected to a suitable etch to allow layer 58 to be inset within layer 204, and layer 202 has not been subjected to such etch. It is to be understood that the invention encompasses other applications (not shown) wherein both of layers 202 and 204 are subjected to the suitable etch to form the inset, as well as other applications in which neither of layers 202 and 204 is subjected to the inset-forming etch. Also, the invention encompasses applications in which layer 202 is subjected to the inset-forming etch and layer 204 is not.

[0073] Referring next to Figs. 38-40, masking layers 210 and 212 (Figs. 35-37) are removed. Such leaves contact pads 234, 235, 236, 237, 238, 239, 240 and 241 where openings 214, 215, 216, 217, 218, 219, 220 and 221, respectively, had previously been.

[0074] Referring next to Figs. 41-43, patterned masks 250 and 252 are formed over layers 202 and 204, respectively, and over contact pads 234, 235, 236, 237, 238, 239, 240 and 241. Masks 250 and 252 can comprise, for example, dry films patterned using photolithographic processing. Masks 250 and 252 define circuit traces. Specifically, masks 250 and 252 cover portions of underlying layers 202 and 204 which are to be incorporated into circuit traces, and leave other portions of layers 202 and 204 exposed.

[0075] Referring next to Figs. 44-46, the exposed portions of layers 202 and 204 are removed, and subsequently patterned masks 250 and 252 (Figs. 41-43) are removed to leave the patterned circuit traces 260 and 262 remaining

over substrate 14. The circuit traces extend to and between conductive pads 234, 235, 236, 237, 238, 239, 240 and 241. The circuit traces also extend between the conductive pads and the vias 206.

[0076] In subsequent processing, not shown, an orifice (or opening) 34 analogous to the orifice described previously with reference to Fig. 24 can be formed across a middle section of substrate 200, and the substrate can then be incorporated into a semiconductor chip package, such as, for example, the package 10 described with reference to Fig. 1. A central region for formation of the orifice is illustrated diagrammatically in Figs. 45 and 46 utilizing the dashed line 290 to demarcate a central region (the region within the dashed line) from a peripheral region (the region outward of the dashed line).

[0077] The various contact pads formed relative to substrate 200 can be utilized in NSMD constructions, and/or SMD constructions. The SMD approach can be more preferred in particular aspects of the invention.

[0078] The processing of Figs. 26-46 has, like the above-described processing of Figs. 10-24, plated contact pads without utilization of prior art busses (such as, for example, the busses 56 described with reference to Figs. 8 and 9). Such can lead to various of the advantages described previously in this disclosure. Among the advantages for eliminating bus lines is that such can eliminate slot burr, and can ease design while saving space and thus allowing a smaller footprint. Additionally, the removal of bus lines from designs of the present products can allow open/short tests to be achieved with the products, and can improve electrical performance at high frequencies due to elimination of an antenna effect caused by bus lines. Wirebondability of bond pads produced in accordance with methodology of the present invention should be similar

regardless of whether electrolytic plating or electroless plating is used. Methodology of the present invention can achieve good plating thickness in relatively short plating time, utilizing electrolytic processes. Etching processes of the present invention can be conducted, in particular aspects, without tail traces left on the pattern.

[0079] Fig. 47 illustrates an exemplary processor system that may include semiconductor components produced using packaging methodology of the present invention, such as, for example, FCIP-BOC, BOC and/or COB packaging. Specifically, a processor system 500 is illustrated which can be, for example, a computer system. The processor system generally comprises a central processing unit (CPU) 502, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 512, 514, and 516 over a system bus 522. System 500 also includes random access memory (RAM) 518, a read-only memory (ROM) 520 and may also include peripheral devices such as a floppy disk drive 504, a hard drive 506, a display 508 and a compact disk (CD) ROM drive 510 which also communicate with the processor 502 over the bus 522. Any or all of the elements of the processor system 500, for example, processor 502, RAM 518, ROM 520 or controller or other IC chips contained within the components shown in Fig. 47 may include semiconductor packages formed using methodology described with reference to Figs. 10-46. It should be noted that Fig. 47 is representative of many different types of architectures of a processor system 500 which may employ the invention. It may also be desirable to integrate the CPU 502 and the RAM 518 on a single chip.

[0080] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to

be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.